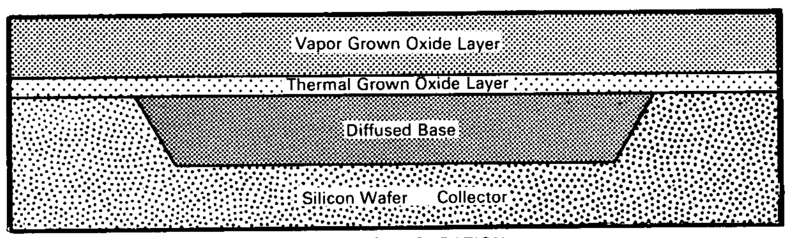
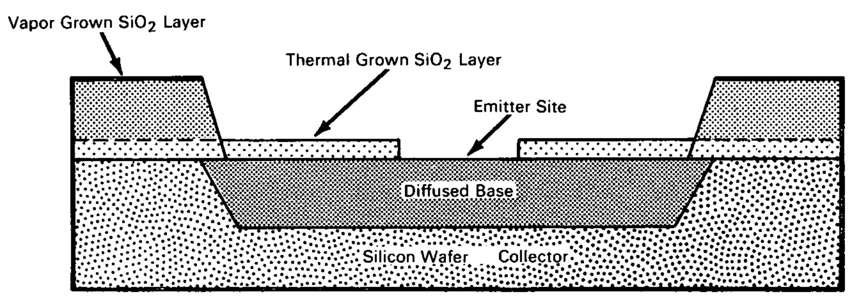
NASA TECH BRIEF

Vapor Grown Silicon Dioxide Improves Transistor Base-Collector Junctions



BASIC CONFIGURATION



FINAL CONFIGURATION

The problem:

To provide greater protection for the base-to-collector junction in silicon planar transistors during the emitter diffusion process. The thermally grown SiO_2 layer normally used to mask the face of the transistor is extremely thin and may have imperfections that could allow the diffusion of impurities into the silicon wafer in the critical junction region.

The solution:

A vapor grown SiO_2 layer covers the entire base-collector junction region. This provides an oxide of greater thickness than can be grown compatible with diffusion times and temperatures and fills in any imperfections that exist in the thermally grown layer.

How it's done:

A portion of the thermally grown SiO_2 layer is selectively removed from the face of the silicon wafer by photoengraving. The base region is than diffused into the silicon wafer and a second thermally grown SiO_2 layer is deposited over the entire face of the assembly. The vapor grown SiO_2 layer is now formed by a chemical reaction with silane (SiH_4) and oxygen at a temperature between 300° and 600°F. Any imperfections that may have existed in the thermally grown layer are filled by the vapor grown layer. The emitter site is next prepared by removal of appropriate portions of the vapor grown and thermally grown dioxide to expose the diffused base region. The vapor grown oxide covers imperfections that may exist in the layer of

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thermally grown oxide in the collector-base region and also prevents penetration to the silicon surface, in critical regions of the junction, of imperfections normally formed during photoengraving of emitter sites. All of the collector-base junction is adequately covered with oxide to prevent penetration of phosphorous during the subsequent emitter diffusion step.

Notes:

1. In laboratory tests, devices prepared by this process were able to deliver 50% efficiency at more than 20 watts of power and a frequency of 430 Mc. Prior devices are limited to 5 watts at such high frequency.
2. This process could be used to deposit protective SiO_2 coatings on optical surfaces.
3. Inquiries concerning this invention may be directed to:

   Technology Utilization Officer
   Goddard Space Flight Center
   Greenbelt, Maryland, 20771
   Reference: B66-10091

Patent status:

Inquiries about obtaining rights for the commercial use of this invention may be made to NASA, Code GP, Washington, D.C., 20546.

Source: Ronald A. Duclos
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of Radio Corporation of America under contract to
Goddard Space Flight Center
(GSFC-389)